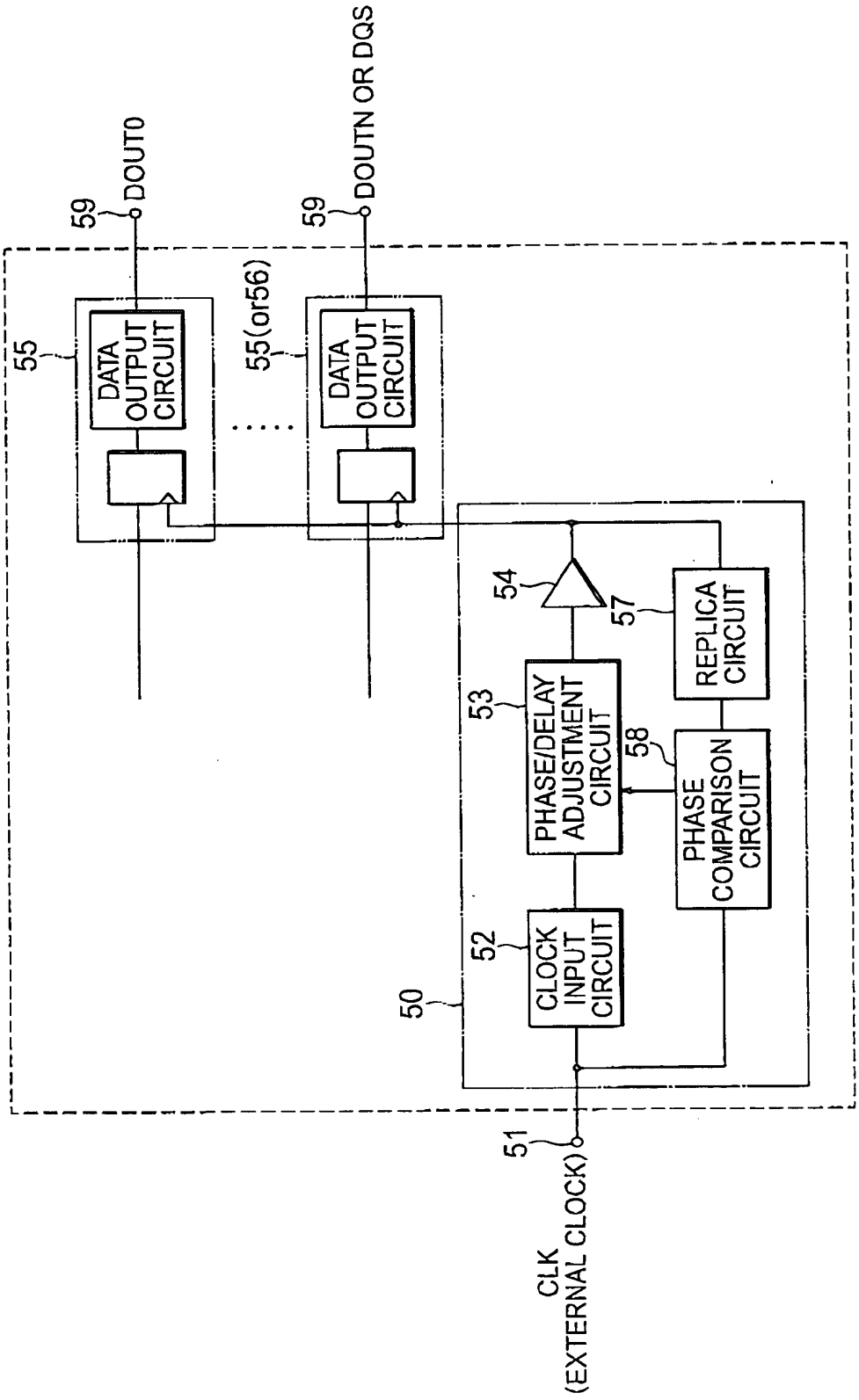

FIG. 1
PRIOR ART

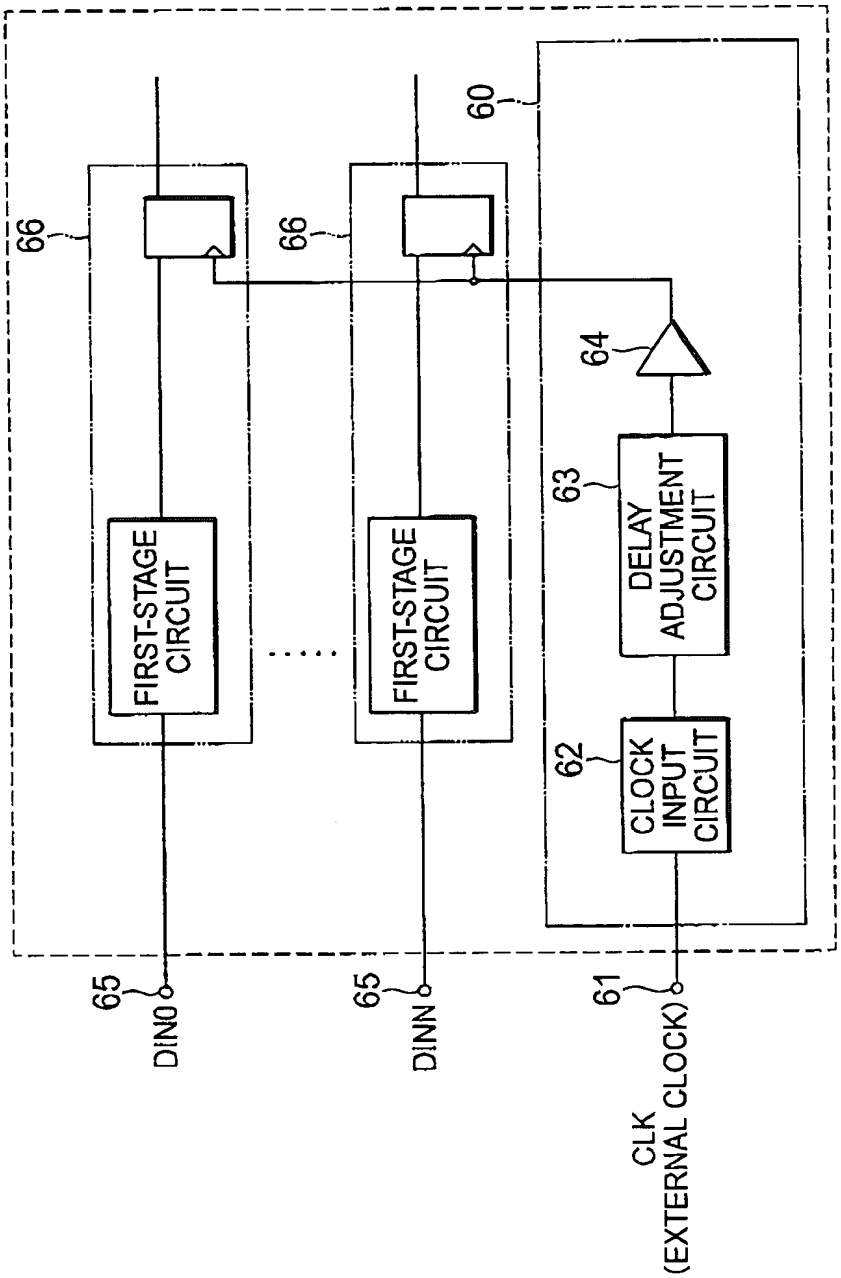

FIG. 2
PRIOR ART

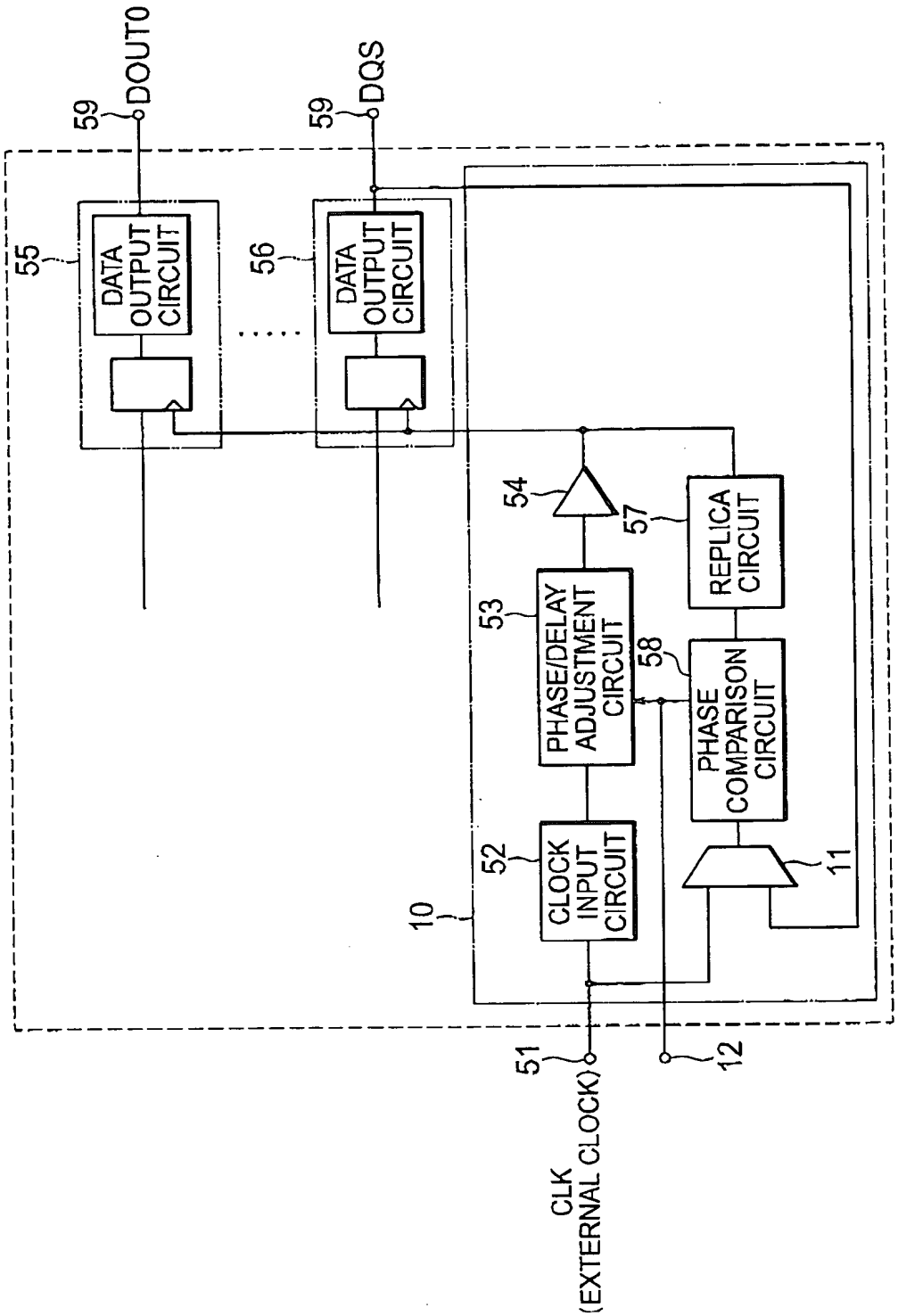
DOUT0
DQS
59
59
55
56
DATA OUTPUT CIRCUIT
DATA OUTPUT CIRCUIT
54
57
REPLICA CIRCUIT
53
PHASE/DELAY ADJUSTMENT CIRCUIT
58
PHASE COMPARISON CIRCUIT
52
CLOCK INPUT CIRCUIT
11
10
51
12
CLK
(EXTERNAL CLOCK)

FIG. 3

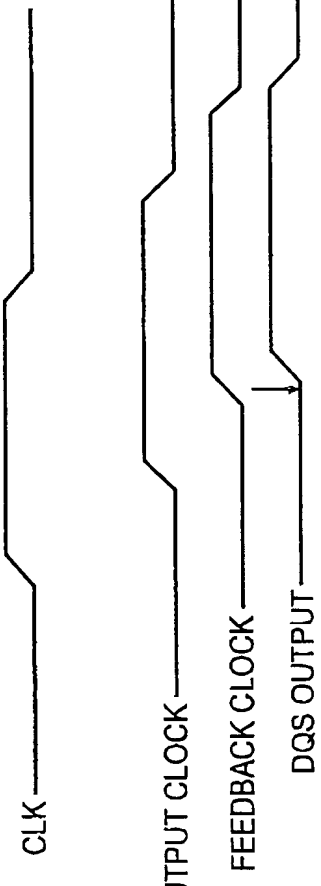
CLK
INTERNAL OUTPUT CLOCK
FEEDBACK CLOCK
DQS OUTPUT

FIG. 4A

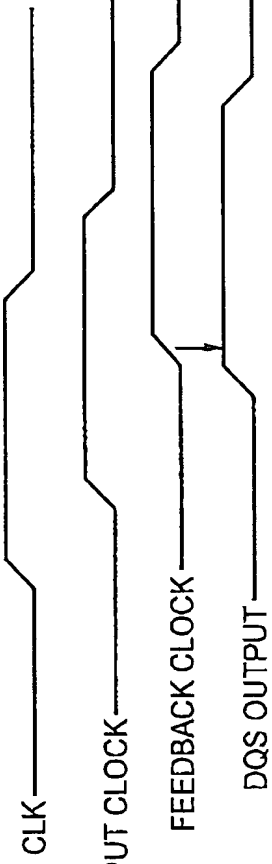
CLK
INTERNAL OUTPUT CLOCK
FEEDBACK CLOCK
DQS OUTPUT

FIG. 4B

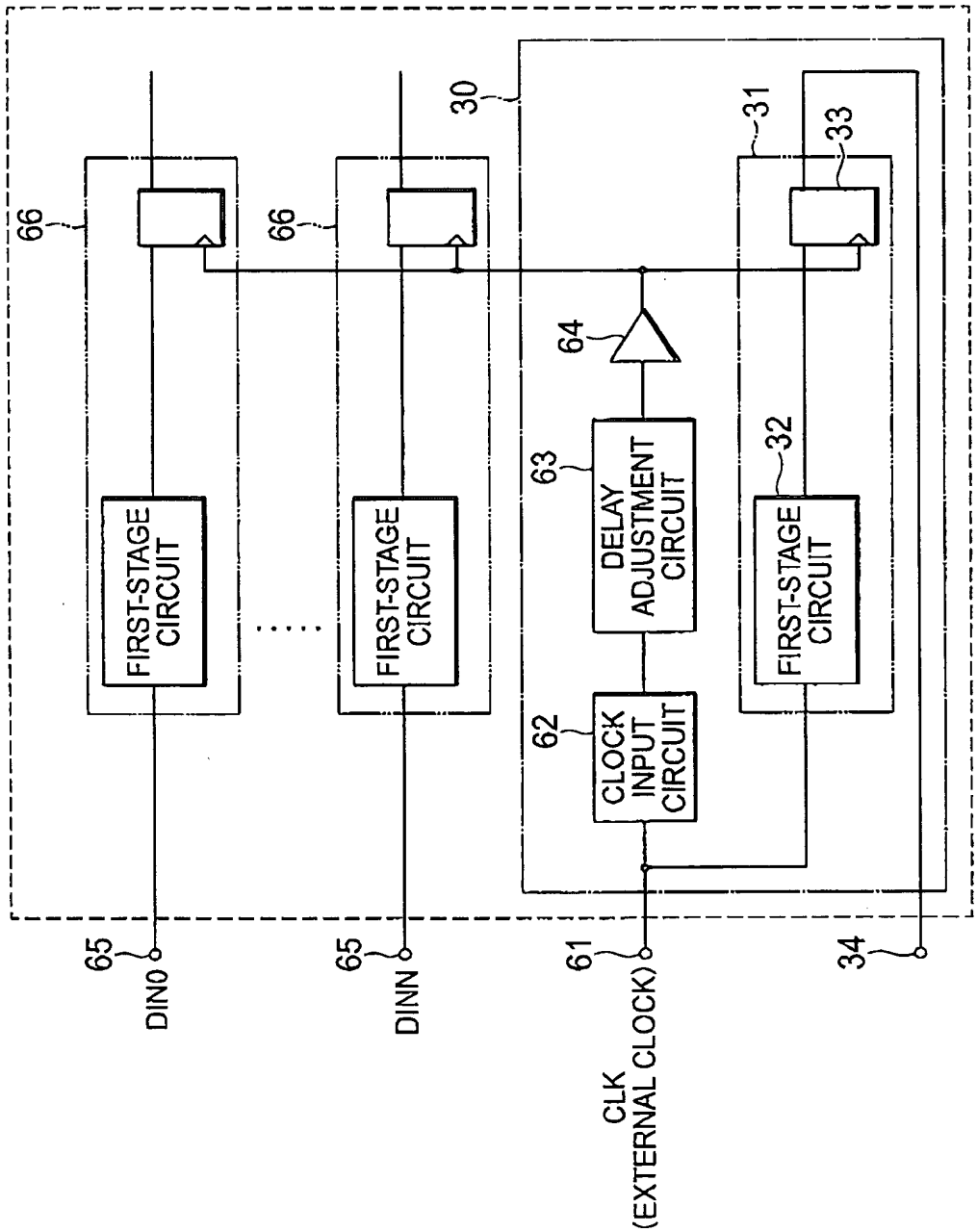
30
31
33
66
66
64
63
DELAY ADJUSTMENT CIRCUIT
32
FIRST-STAGE CIRCUIT
FIRST-STAGE CIRCUIT
FIRST-STAGE CIRCUIT
62
CLOCK INPUT CIRCUIT
65
DIN0
65
DINN
61
CLK (EXTERNAL CLOCK)
34

FIG. 5

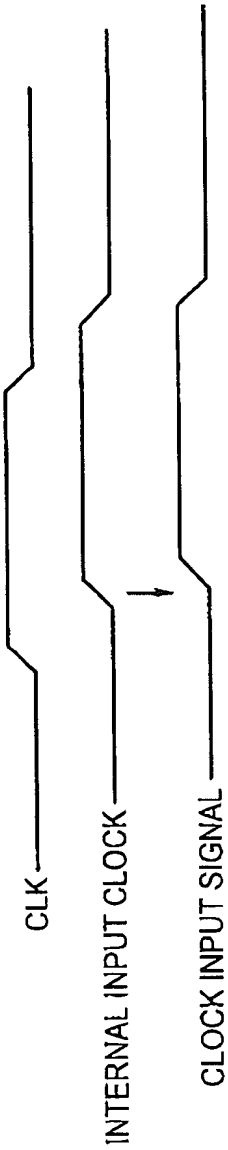
CLK
INTERNAL INPUT CLOCK
CLOCK INPUT SIGNAL

FIG. 6A

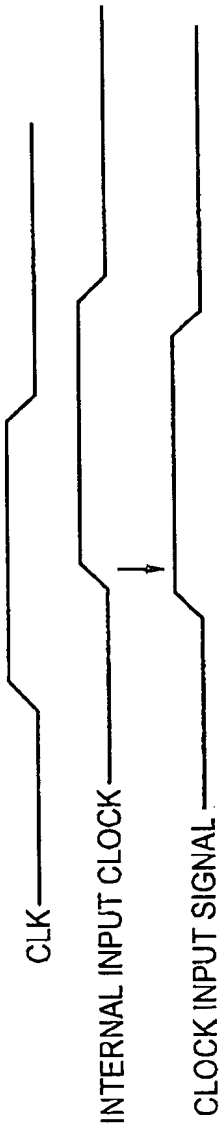
CLK
INTERNAL INPUT CLOCK
CLOCK INPUT SIGNAL

FIG. 6B